# XA-160M

**PCI Express XMC Module with Two 160 MSPS A/Ds, Two 615 MSPS DACs and Artix-7 FPGA** V1.2

## FEATURES

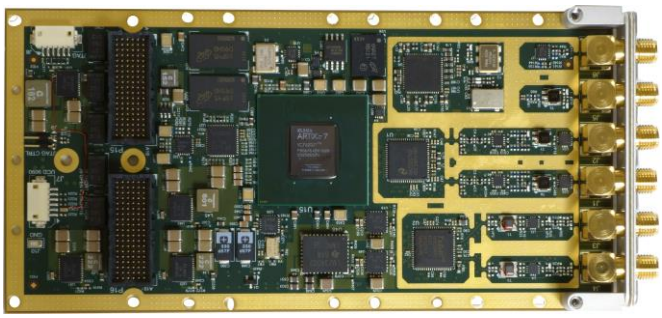
- Two 160 MSPS, 16-bit ADC channels
- Two 615 MSPS, 16-bit DAC channels
- Up to 89 dB SFDR, 72 dBFS SNR A/Ds
- Up to 76 dB SFDR, 66 dBFS SNR D/As
- 2.4Vpp input range
- 1Vpp output range
- DIO on P16 (19 differential pairs)
- Xilinx Artix-7 FPGA
- DDR3 Memory
- Programmable or external sample clock
- Synchronized system sampling using common reference clock and triggers
- Framed, software or external triggering
- Log acquisition timing and events
- Power management features
- PCI Express 2.0 XMC Module (75x150 mm)
- Use in any PCI Express desktop, compact PCI/PXI, PXIe, or cabled PCI Express application

## APPLICATIONS

- Stimulus-response measurements
- High speed servo controls
- Arbitrary waveform generation

## SOFTWARE

- Data Acquisition, Logging and Analysis applications provided
- Windows/Linux Drivers
- C++ Host Tools
- VHDL



The XA-160M is an XMC IO module featuring two 16-bit, 160 MSPS A/D channels and two 16-bit, 615 MSPS DAC channels designed for high speed stimulus-response, ultrasound, and servo control applications.

Flexible trigger methods include counted frames, software triggering and external triggering. The sample rate clock is either an external clock or on-board programmable PLL clock source.

Data acquisition control, signal processing, buffering, and system interface functions are implemented in a Xilinx Artix-7 FPGA device. Two 256Mx16 memories provide data buffering and FPGA computing memory.

The logic can be fully customized using VHDL using the FrameWork Logic toolset.

The PCI Express 2.0 interface supports data rates up to 1600 MB/s for unbuffered continuous data or burst data streams. When using a standard configuration involving DDR3 buffered data, a continuous data rate up to 1300 MB/s is supported.

# XA-160M

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Interconnect Systems International, LLC standard warranty. Production processing does not necessarily include testing of all parameters.

This electronics assembly can be damaged by ESD. Interconnect Systems International, LLC recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| **Product** | Part Number | Description |
|---|---|---|
| XA-160M | 80362-0-L0<br>80362-1-L0<br>80362-10-L0<br>80362-11-L0 | XMC module with two 160 MSPS A/D, two 615 MSPS DACs, Artix-7 FPGA<br>XA-160M with Artix-7 FPGA AC-COUPLED<br>XA-160M with Artix-7 FPGA DC-COUPLED<br>XA-160M with Artix-7 FPGA AC-CPLD HTSK<br>XA-160M with Artix-7 FPGA DC-CPLD HTSK |
| | | |
| **Logic** | | |
| FrameWork Logic | 55050 | XA-160M FrameWork Logic board support package for RTL. Includes technical support for one year. |
| **Cables** | | |
| SMA to BNC cable | 67048G | IO cable with SMA (male) to BNC (female), 1 meter |
| **Adapters** | | |
| XMC-PCIe x8 Lane | 80363-2-L0<br>80363-3-L0 | XMC-PCIe X8 ADAPTER XMC INT PWR<br>XMC-PCIe X8 ADAPTER XMC EXT PWR |
| XMC-PCIe x8 Lane Legacy | 80173-0 | PCIe-XMCe 8 LANE ADAPTER BRD |
| XMC-PXIe x8 Lane | 80341-1-L0 | XMC-PXIE Adapter X6 3U 8HP |
| **Embedded PCs** | | |
| ePC-Duo | 90602<br>See datasheet for options | ePC-Duo, Skylake Processor, 32GB RAM, x1 Gbe, x2 10 Gbe, x4 mSATA, x2 QSFP ports, onboard USB JTAG interface, Single Ended/Differential, LMK04828/LMK04821, GPS/IEEE/NO TIMING MOD, High Quality DIO. |
| SBC-Nano | 90654-0-L0 | SBC-Nano: Carrier Board for x1 XMC module, COM Express Type 10 ATOM, 8 GB DDR3L memory, x4 lanes PCIe, x2 mSATA, x1 Gbe, Conduction or Convection cooled chassis |

# XA-160M

## BLOCK DIAGRAM

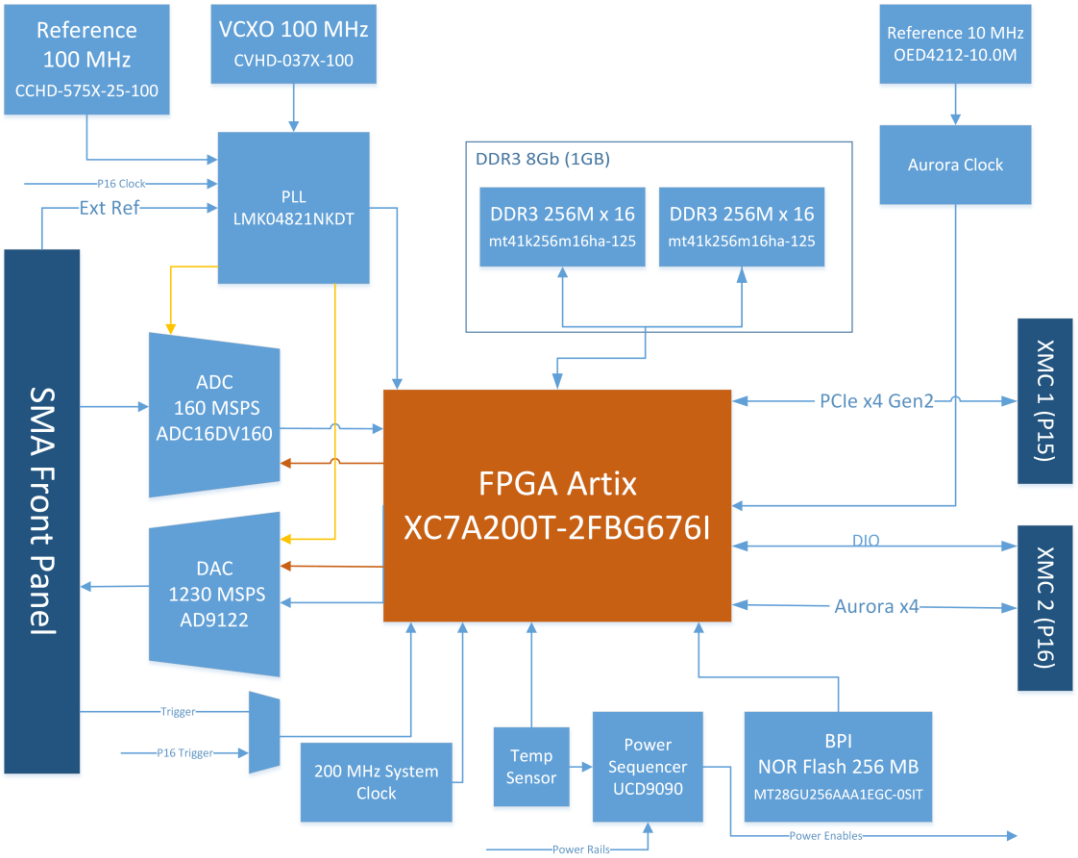




**Illustration 1: Connections available on XA-160 front panel**

# XA-160M

INTERCONNECT SYSTEMS
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## Standard Features

| Analog | |
|---|---|
| Inputs | 2 |
| Input Ranges | ±1.2V |
| Input Type | Single ended, AC or DC coupled |
| Input Impedance | 50 ohm |
| A/D Device | Texas Instruments ADC16DV160 |
| A/D Resolution | 16-bit |
| A/D Sample Rate | Up to 160 MHz<br>** Decimation feature in logic used for lower data rates |
| A/D Latency | 11.5 clock cycles |
| Outputs | 2 |
| Output Range | ±0.5V |
| Output Type | Single ended, AC or DC coupled |
| Output Impedance | 50 Ohm |
| DAC Device | Analog Devices AD9122 |
| DAC Resolution | 16-bit |
| DAC Latency | 64 clock cycles |
| DAC Sample Rate | Up to 615 MHz |
| Data Format | 2's complement, 16-bit integer |
| Connector | SMA |
| Calibration | Factory calibrated. Gain and offset errors are digitally corrected in the FPGA. Non-volatile EEPROM coefficient memory. |

| Memory | |
|---|---|
| Size | 2 devices @ 256Mx16 each |
| Type | DDR3 |
| Uses | FPGA Buffer Memory<br>FPGA computation memory |

| Clocks and Triggering | |
|---|---|
| Clock Sources | Internal 100 MHz 50ppm reference or external |
| Input Type | Single ended, AC coupled |
| External Clock Input Range | 0.25 – 3.1 Vpp |
| External Trigger Input Range | 1.3 – 2.5 Vpp (centered at 1.25V) |
| Input Impedance | 50 ohm |

| FPGA | |
|---|---|
| Logic Cells | 215360 |
| Slices | 33650 |
| Block RAM | 13,140Kb Max |
| DSP Slices | 740 |
| FPGA Device | Xilinx Artix-7<br>XC7A200T-2FBG676I |
| Configuration | SelectMAP from PCIe interface<br>JTAG during development |
| Clock Speed | 250 MHz |

# XA-160M

INTERCONNECT SYSTEMS
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| Host Interface | |
|---|---|
| Type | PCI Express 2.0 four lane |
| Sustained Data Rate | 1300 MB/s (DDR3 Max) |
| Protocol | Packet data |
| Connector | XMC P15, P16 |
| Interface Standard | PCIe 2.0 |
| Logic Update | In-system reconfiguration |

| Clocks and Triggering | |
|---|---|
| Clock Sources | PLL or External |
| PLL Output | 44 KHz to 2000 MHz |
| PLL Jitter | <1 ps RMS |
| PLL Programming | Host programmed via PCIe |
| PLL Reference | Internal: 100 MHz clock<br>External reference: J16 input |
| Triggering | External, software, acquire N frame |
| Decimation | 1:1 to 1:4095 in FPGA |
| Channel Clocking | All channels are synchronous |
| Multi-card Synchronization | External triggering, clock, and PLL reference are supported. |

| Acquisition Monitoring | |
|---|---|
| Alerts | Trigger, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure, PLL Unlocked |
| | |

| P16 Digital IO | |
|---|---|
| Total Number of Bits | 36 |
| Balanced Pairs | 18 |
| DIO is 4 pairs in the same FPGA banks as the ADC and 13 pairs in a separate FPGA bank | |
| Signal Standard | LVCMOS 2.5V |
| Drive | ±12 mA |
| Connector | XMC P16 |

| Power Management | |
|---|---|
| Temperature Monitor | May be read by the host software |
| Alarms | Software programmable warning and failure levels |
| Over-temp Monitor | Disables analog IO power supplies |
| Power Control | Channel enables and power up enables |
| Heat Sinking | Conduction cooling supported.(subset of VITA20) |

| Physicals | |
|---|---|
| Form Factor | Single width IEEE 1386 Mezzanine Card |
| Size | 75 x 150 mm |
| Weight | TBD |
| Hazardous Materials | Lead-free and RoHS compliant |

# XA-160M

| ABSOLUTE MAXIMUM RATINGS<br><br>Exposure to conditions exceeding these ratings may cause damage! In general, unit is not guaranteed to function under these conditions. | | | | |
|---|---|---|---|---|
| Parameter | Min | Max | Units | Conditions |
| Supply Voltage, 3.3V to GND | 0 | +3.6 | V | |
| Supply Voltage, VPWR to GND | 0 | 14 | V | |
| Operating Temperature | 0 | 70 | C | Non-condensing, forced air cooling required |
| Storage Temperature | -40 | 100 | C | |
| ESD Rating | - | 2k | V | Human Body Model |
| Vibration | - | 5 | g | 9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04) |
| Shock | - | 40 | g peak | Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04) |

| RECOMMENDED OPERATING CONDITIONS | | | | |
|---|---|---|---|---|
| Parameter | Min | Typ | Max | Units |
| Supply Voltage | 3.15 | +3.3 | +3.45 | V |
| Supply Voltage, Nominal 12V VPWR | 11.4 | 12 | 12.6 | V, unless otherwise noted specified and tested with nominal 12V VPWR |
| A/D Sampling Rate | 1 | | 160 | MSPS |
| DAC Update Rate | 0 | | 615 | MSPS |
| Operating Temperature | 0 | | 50 | C (Note 1) |

Notes:

1. Unit will operate properly up to 70° C, but operating life may be impaired.

# XA-160M

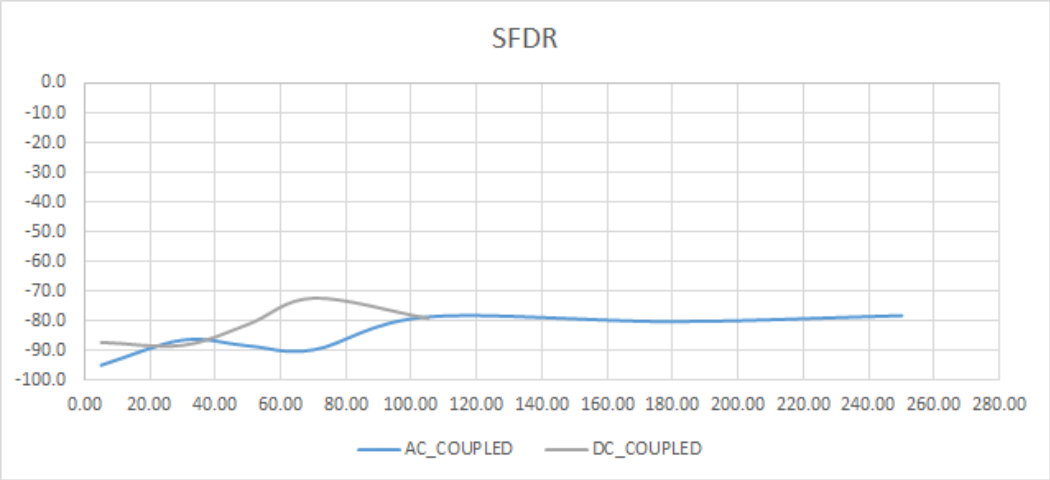
| | **ELECTRICAL CHARACTERISTICS**<br>Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted. | | | | |
|---|---|---|---|---|---|
| **Group** | **Parameter** | **Cfg.** | **Typ** | **Units** | **Notes** |
| Analog Inputs | -3dB Bandwidth | -0 | 0.1 - 350 | MHz | AC coupled |
| | | -1 | 0 - 160 | MHz | DC coupled |
| | SFDR | -0 | 95 | dB | AC coupled, 5.1 MHz input, FS = 159 MSPS |
| | | -1 | 87 | dB | DC coupled, 5.1 MHz input, FS = 159 MSPS |
| | SNR | -0 | 76 | dB | AC coupled, 5.1 MHz input, FS = 159 MSPS |
| | | -1 | 74 | dB | DC coupled, 5.1 MHz input, FS = 159 MSPS |
| | THD | -0 | -91 | dB | AC coupled, 5.1 MHz input, FS = 159 MSPS |
| | | -1 | -84 | dB | DC coupled, 5.1 MHz input, FS = 159 MSPS |
| | ENOB | -0 | 12.4 | Bits | AC coupled, 5.1 MHz input, FS = 159 MSPS |
| | | -1 | 12.0 | Bits | DC coupled, 5.1 MHz input, FS = 159 MSPS |
| | Channel Crosstalk | All | < -109 | dB | 70 MHz input, FS = 125MSPS, 98% FS. Adjacent Channel |
| | Noise Floor | All | < -115 | dB | |
| | Gain Error | All | < 0.5 | % of FS | Calibrated |
| | Offset Error | All | < 500 | uV | Calibrated |
| Analog Outputs | Analog Output Range | All | ±500 | mV | Typical, AC and DC Coupled |
| | Analog Output Bandwidth | All | 615 | MHz | AC and DC Coupled, no sinc compensation |

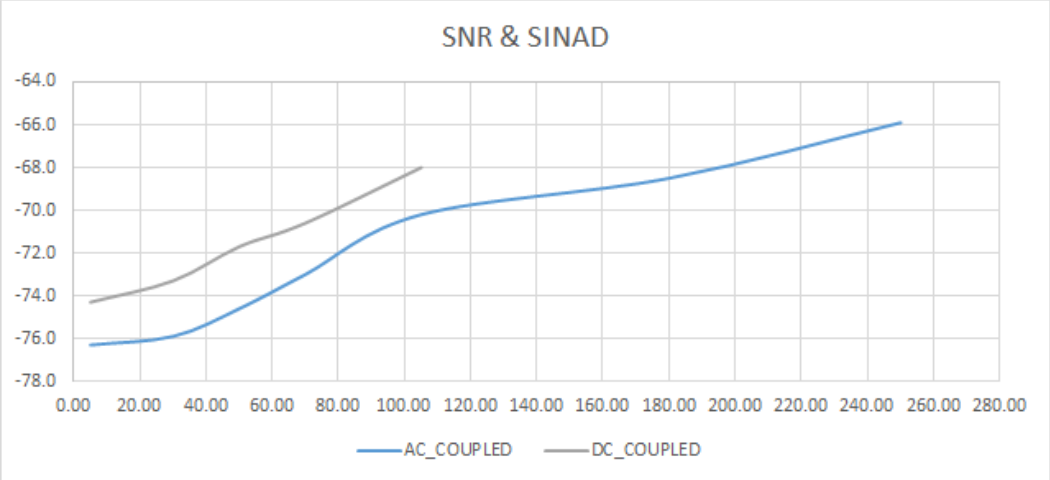
# XA-160M

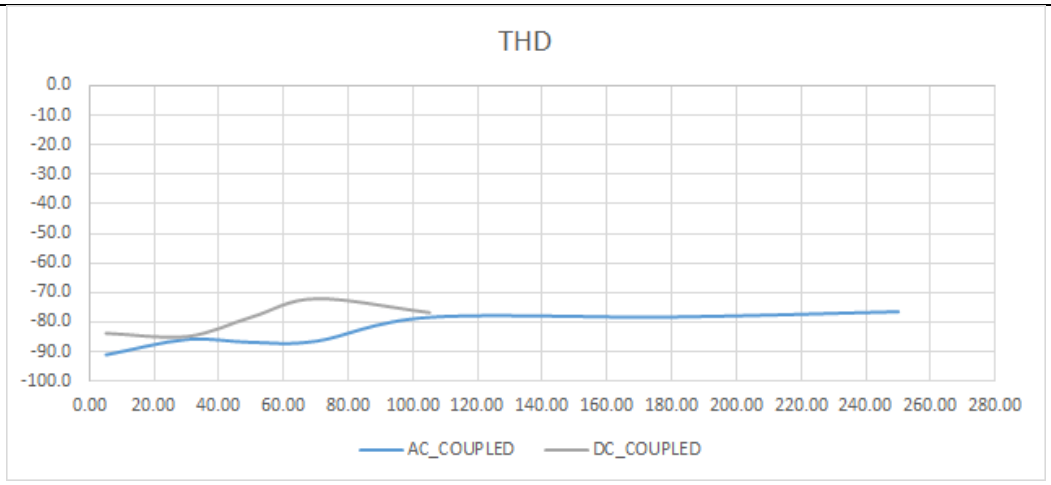
| | | | | | |
|---|---|---|---|---|---|
| | **ELECTRICAL CHARACTERISTICS**<br>Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted. | | | | |
| | SFDR | -0 | 76 | dB | 1-100 MHz, AC Coupled, no sinc compensation |
| | | -1 | 68 | dB | 0-100 MHz, DC Coupled, no sinc compensation |
| | SNR | -0 | 66 | dB | 20 MHz sine output, 95% FS, AC coupled |
| | | -1 | 69 | dB | 20 MHz sine output, 95% FS, DC coupled |
| Power | Supply Current | All | 3.5 | A | Max |
| | Power Dissipation | All | 17 | W | Max |

# XA-160M

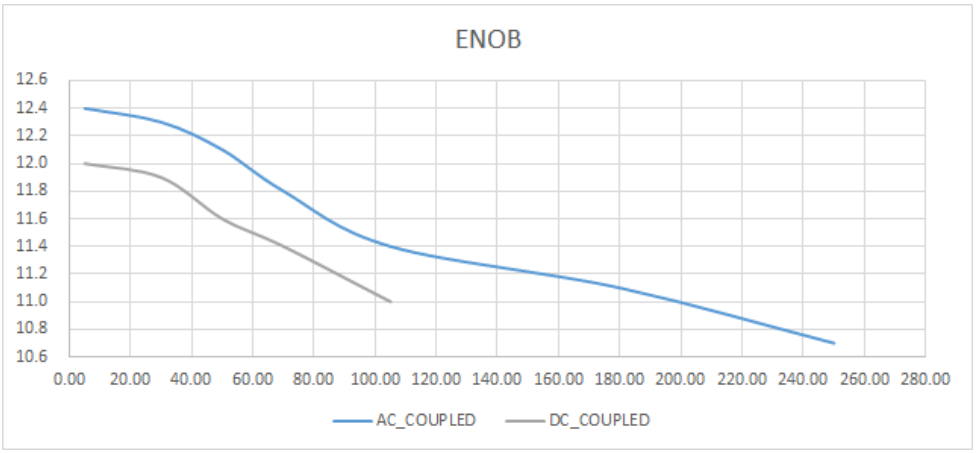
**Typical ADC Performance**





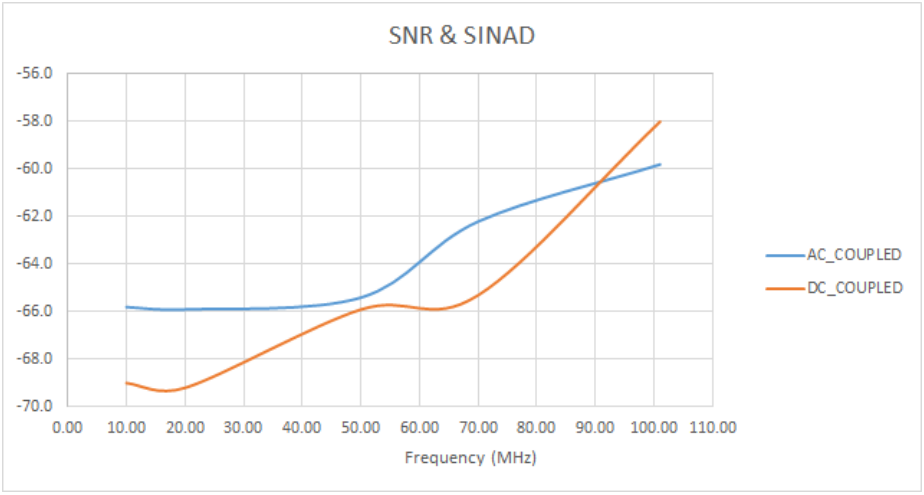

**Typical ADC Performance Continued**

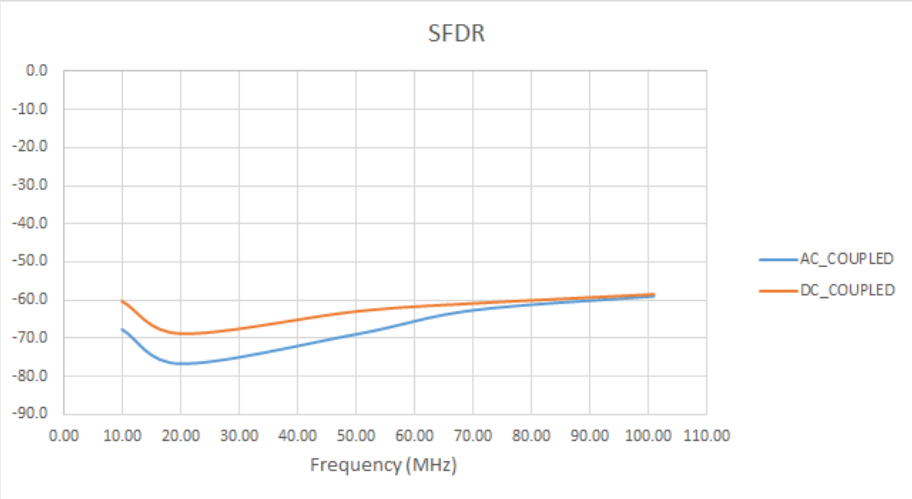



| ADC AFE Delay | |
|---|---|
| Frequency (Mhz) | Delay (nS) |
| 160 | 0.3 |
| 100 | 0.3 |
| 70 | 0.3 |
| 20 | 0.5 |
| 1 | 2 |

# XA-160M

**Typical DAC Performance**






| DAC AFE Delay | |
|---|---|
| Frequency (Mhz) | Delay (nS) |
| 160 | 1.5 |
| 100 | 2.75 |
| 70 | 3 |
| 20 | 6.25 |
| 1 | 10 |

# XA-160M

## Architecture and Features

The XA-160M module has two analog inputs that are simultaneously sampling channels of 16-bit, 160 MSPS A/D input and two analog output channels of 615 MSPS, 16-bit D/A converter. The A/D inputs have an input bandwidth of 350MHz for AC coupled and 160MHz for DC coupled. The two DAC channels have a ±1V output range. Additional digital IO control bits from the FPGA are provided for application control and signaling.

Controls for triggering and clocks allow precise control over the collection of data. Trigger modes include frames of programmable size, external and software. Multiple XA-160M cards can sample simultaneously using external trigger inputs with synchronized sample clocks. The sample clock can be external or generated from the on-card PLL. The PLL can either use the on-card 100 MHz reference, or can use an external reference. When an external reference is used, the sample clock is synchronous to the reference.

The XA architecture has a data buffering and packet system that provides efficient and flexible data transfers to the host computer. The data buffer uses the entire SDRAM memory in a single virtual FIFO mode. Data from both ADCs are interleaved into a single stream. Data is transferred to the host using the PCIe controller interface as data packets. The packet data system controls the flow of packets to the host, or other recipient, using a credit-based system managed in cooperation with the host software. The packets may be transmitted continuously for streams of data from the A/Ds, or as occasional packets for status, controls and analysis results. The data buffering and flow control system delivers high throughput with low latency and complete flexibility for data types and packet sizes to match the application requirements for all types of applications.

The data acquisition process can be monitored using the XA alert mechanism. The alerts provide information on the timing of important events such as triggering, overranges and thermal overload. Packets containing data about the alert including an absolute system timestamp of the alert, and other information such as current temperature. This provides a precise overview of the card data acquisition process by recording the occurrence of these real-time events making the XA modules easier to integrate into larger systems.

## Software Tools

Software for data logging and analysis are provided with every XA module. Data can be logged to system memory at full rate or to disk at rates supported by the drive and controller. Triggering, sample rate controls, and data logging features allow you to use XA modules in your application without ever writing code. Our software applications include *Binview* program which provides data viewing, analysis, and export data to MATLAB for large data files, as well as support applications for logic loading, firmware updates, and system configuration.

Software development tools for the XA modules provide comprehensive support including device drivers, data buffering, card controls, and utilities that allow developers to be productive from the start. At the most fundamental level, the software tools deliver data buffers to your application without the burden of low-level real-time control of the cards. Software classes provide C++ developers a powerful, high-level interface to the card that makes real-time, high-speed data acquisition easier to integrate into applications. By default, Qt-Creator project files are provided to compile and build C/C++ applications on 64bit

Windows or Linux operating systems. For additional support please contact ISITechSupport@molex.com.

## Logic Tools

High speed DSP, analysis, customized triggering and other unique features may be added to the XA modules by modifying the logic. The FrameWork Logic tools support RTL developments. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designer can build upon the Framework Logic components for packet handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is available for customization. Contact ISISales@Molex.com. Each design is provided as a Xilinx Vivado project.

The FrameWork Logic User Guide more fully details the development tools.

# XA-160M

## Applications Information

### Maximum Data Rates

The maximum data rates supported by the module are limited by the DDR3 memory transfer rate when the total data rate exceeds 1300 MB/s. The PCI Express transfer rate can reach up to 1600MB/s which allows full saturation of the DDR3 rate. The XA-160M modules supports 2600 MB/s full duplex data flow, which is within the capability of the PCIe interface.

**It is important to qualify systems for performance when data rates exceeding 1300 MB/s are required.**

### Cables

The XA-160M module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SMA male connector and 50-ohm characteristic impedance for best signal quality.

# XA-160M

## XMC Adapter Cards

XMC modules can be used in standard desktop system or compact PCI/PXIe using an adapter card. The adapter cards are software transparent.

The XA modules use the auxiliary P16 connector for digital IO and additional clock inputs. A total of 8 bits of digital IO, directly connected to the application FPGA, are routed to the J16 connector as 4 balanced differential pairs supporting LVDS or lower speed single-ended LVCMOS signals. The XA modules also have a sample clock input and PLL reference input to J16. The cPCI/PXIe adapter uses these to connect to system clocks, while the PCIe desktop adapter provides SMB input connectors for system clock inputs.

| | | |
|---|---|---|
| **PCIe-XMC Adapter (80341)**<br>x8 PXIe to XMC<br>Clock and trigger inputs | **PCIe-XMC Adapter (80260)**<br>x8 VPX to XMC<br>Conduction cooling | **ASSY XMC-PCIe x8 ADAPTER (80363)**<br>x8 PCIe to XMC<br>On-board USB to JTAG Programmer<br>High speed expansion port (Mini-SAS, QSFP)<br>Conduction Cooling<br>External VPWR Power option available<br>XMC Module Voltage and Current Test Header |
|  |  |  |
| **PCIe-XMC Adapter x8 lane (80173)**<br>x8 PCIe to XMC<br>P16 x8 RIO ports to SATA2 connectors<br>DIO to MDR68 | | |
|  | | |

# XA-160M

Applications that need remote or portable IO can use either the ePC-Duo or eInstrument Node with XA modules.

| | |
|---|---|
| **ePC-Duo (90602)**<br>Windows/Linux embedded PC<br>8x USB, GbE, cable PCIe, VGA<br>High speed x8 interconnect between modules<br>GPS disciplined, programmable sample clocks and triggers to XMCs<br>2000 MB/s, 4 TB datalogger<br>9-18V operation | **SBC-Nano (90654-0-L0)**<br>Windows/Linux Embedded Single Board Computer<br>Extremely small form-factor<br>Single XMC IO Site and 1 GbE Link<br>8-14Vdc operation |
|  |  |

## Usage and Market

The XA-160M is a digital device and apparatus exclusively for use in business, industrial and commercial environments. The XA-160M peripheral is not marketed, sold or otherwise made available for home or residential environment use.

The XA-160M is exclusively for use with wired input and output signals. The XA-160M peripheral is not an intentional radio transmitter or receiver and is not marketed, sold or otherwise made available for connection to wireless media (with an antenna, etc…).

The XA-160M is not a “PC” (“personal” or “portable computer” marketed for home or residential environment use) or “PC” peripheral and is not marketed, sold or otherwise made available as a “PC” or “PC” peripheral.

The XA-160M may be sold as a subassembly where the integrator/purchaser takes responsibility for their assembled digital device’s or apparatus’s compliance. Consult Molex for clarification and assistance.

## Compliance

The product herewith complies with the requirements of the Low-Voltage Directive 2014/35/EU, the EMC Directive 2014/30/EU

# XA-160M

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# XA-160M

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