



XMC Adapter for 3U OpenVPX



Rugged Conduction or Air Cooled XMC Adapter with IPMI Support

V 1.1 11/30/11

FEATURES

- Adapt one XMC module to a 3U OpenVPX VITA 65 system
- VITA42 XMC site
- VITA65 OpenVPX compatible
- Configurable mapping for VPX to XMC communications ports
- Configurable Digital IO with VITA 46.9 maps
 - XMC P16 mapped as X38s
 - XMC JN4 mapped as P64s
- System management using IPMI
 - Dual SMB buses
 - Power, temperature monitoring
- Extended environment ratings
 - -40 to +85C operation
 - 40g shock
 - 0.1 g²/Hz random vibration
- Conduction cooling
 - Heat-spreading frame with direct path to host
 - VITA20 conduction cooling
- Air Cooling
 - flow-through air path
 - heat-spreading for improved convection effectiveness
- Supports 0.8 inch slot spacing
- 2 level maintenance RED! covers available

SOFTWARE

- No software required
- Transparent operation



XMC-VPX Adapter



VPX-XMC Conduction-Cooled Adapter Assembly

DESCRIPTION

The VPX-XMC module adapter allows a single width XMC module to be used in a 3U OpenVPX slot. The adapter is available in either conduction-cooled or air-cooled models.

The VPX-XMC adapter is designed for use in harsh environments. Environmental ratings for temperature, vibration and shock are available for demanding in military, heavy industry, and aerospace applications.

The adapter has configurable port mappings between the XMC and the VPX host ports A through D. This flexible mapping allows the XMC module to work with a variety of system topologies and backplanes.

Digital IO from the XMC is mapped to backplane connector P2 from either J16 or Jn4 according to VITA 48.10 standard. The mapping is jumper selectable on the adapter. Optional connections for trigger and clock features for X3 and X6 module families are provided.

No software is required to operate the adapter unless IPMI functions are required. All configurations may be set without IPMI. Applications requiring system management functions for health monitoring and control use the IPMI interface, an independent dedicated processor on the card.

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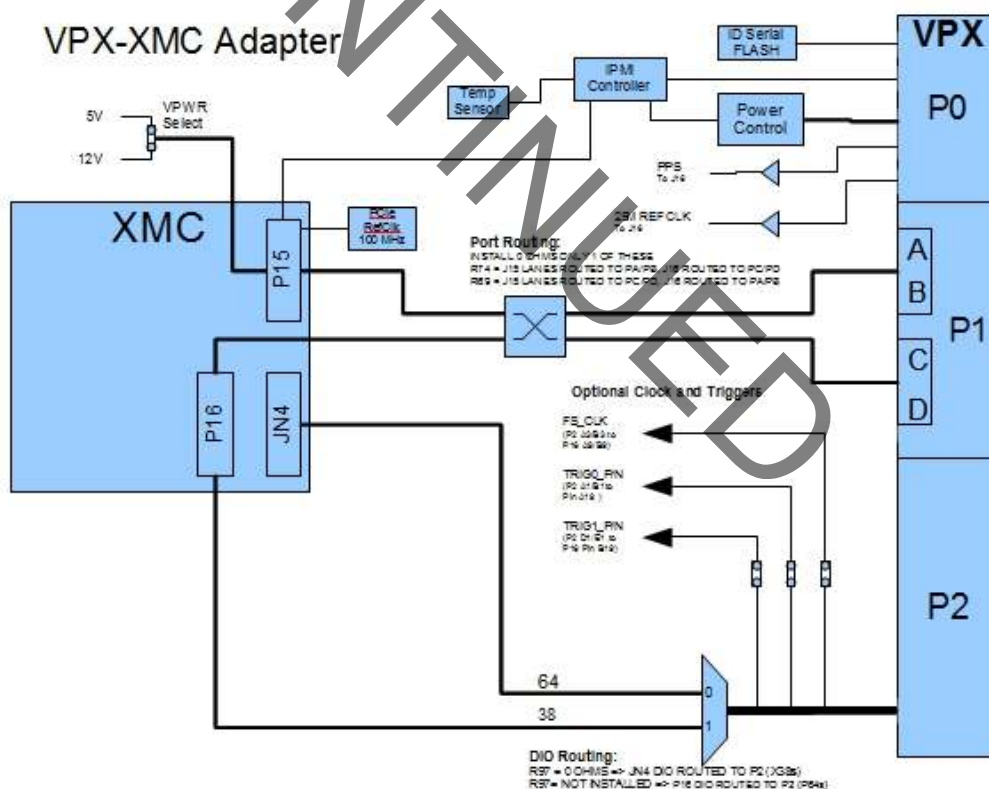


This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part Number	Description
VPX-XMC Adapter	80260-0-<er>	VPX-XMC Adapter, air-cooled with REDI covers, no IPMI functions
VPX-XMC Adapter	80260-1-<er>	VPX-XMC Adapter, conduction-cooled without REDI covers for generic XMC, no IPMI functions
VPX-XMC Adapter	80260-3-<er>	VPX-XMC Adapter, conduction-cooled without REDI covers for X3 family XMC, no IPMI functions
VPX-XMC Adapter	80260-5-<er>	VPX-XMC Adapter, conduction-cooled without REDI covers for X5 family XMC, no IPMI functions
VPX-XMC Adapter	80260-6-<er>	VPX-XMC Adapter, conduction-cooled without REDI covers for X6 family XMC, no IPMI functions
X3 REDI Covers	61209-3	REDI covers for X3 modules, primary and secondary, screws
X5 REDI Covers	61209-5	REDI covers for X5 modules, primary and secondary, screws
X6 REDI Covers	61209-6	REDI covers for X6 modules, primary and secondary, screws

-<er> is environment rating; see table



XMC Adapter for 3U OpenVPX

Operating Environment Ratings

VPX-XMC adapters are rated for operating environment temperature, shock and vibration are offered. The assemblies are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance.

Environment Rating <ER>		L0	L1	L2	L3	L4
Environment		Office, controlled lab	Outdoor, stationary	Industrial	Vehicles	Military and heavy industry
Applications		Lab instruments, research	Outdoor monitoring and controls	Industrial applications with moderate vibration	Manned vehicles	Unmanned vehicles, missiles, oil and gas exploration
Cooling		Forced Air, 2 CFM	Forced Air, 2 CFM	Conduction	Conduction	Conduction
Operating Temperature		0 to +50C	-40 to +85C	-20 to +65C	-40 to +70C	-40 to +85C
Storage Temperature		-20 to +90C	-40 to +100C	-40 to +100C	-40 to +100C	-50 to +100C
Vibration	Sine	-	-	2g 20-500 Hz	5g 20-2000 Hz	10g 20-2000 Hz
	Random	-	-	0.04 g ² /Hz 20-2000 Hz	0.1 g ² /Hz 20-2000 Hz	0.1 g ² /Hz 20-2000 Hz
Shock		-	-	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity		0 to 95%, non-condensing	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Conformal coating			Conformal coating	Conformal coating, extended temperature range devices	Conformal coating, extended temperature range devices, Thermal conduction assembly	Conformal coating, extended temperature range devices, Thermal conduction assembly, Epoxy bonding for devices
Testing		Functional, Temperature cycling	Functional, Temperature cycling, Wide temperature testing	Functional, Temperature cycling, Wide temperature testing, Vibration, Shock	Functional, Temperature cycling, Wide temperature testing, Vibration, Shock	Functional, Testing per MIL-STD-810G for vibration, shock, temperature, humidity

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

XMC Adapter for 3U OpenVPX

Physicals	
Form Factor	3U
Size	160 x 100mm 6.30 x 3.94 in
Slots	0.80 in minimum slot width
Weight	100g (air-cooled, no REDI covers) 300g (conduction-cooled with REDI covers)

XMC Site	
Form Factor	75x150 mm modules (IEEE 1386)
Mounting height	10mm for single slot
Specification	VITA 42
Communications Interfaces	16 lanes total J15 : 8 lanes, J16: 8 lanes
PCI Express Ref Clock	100 MHz, Gen2 compatible

Power Delivered to the XMC**	
Volts	Amps
3.3V	6A Max
VPWR = 5V or 12V (selectable)	5V : 6A Max 12V : 3.3A Max
3.3V AUX	0.5A

** Check host system power capabilities for other limitations.

VPX Interface	
Specification	VITA65 OpenVPX
Lanes (Rx/Tx pair)	16 total (P1 ports A,B,C,D)
Speed	5 Gbps max
Routing to XMC	Jumper selectable routing for J15 and J16 routing to Ports A,B,C,D
Digital IO	Jumper selectable routing for XMC J16 or JN4 to P2. VITA46.9 mapping : X38s or P64s Routed as differential pairs, length matched

System Management (IPMI) Option	
SMB Buses	2; Connect to IPMI processor
IPMI Processor	Atmel ATMega128
ROM	IPMI v2.0
Monitoring	Board temperature Power supplies (3.3V, 5V, +12V) power good indicator and voltage
Indicators	LEDs: Red, Green, Blue
XMC connection	UART (2 wire)
Reset Control	Can reset XMC module

Optional Triggering and Clocking Features	
Trigger inputs	2 LVDS differential pairs LVCMOS inputs to XMC Jumper selectable
Clock Inputs	1 differential pair, 50 ohm Jumper selectable

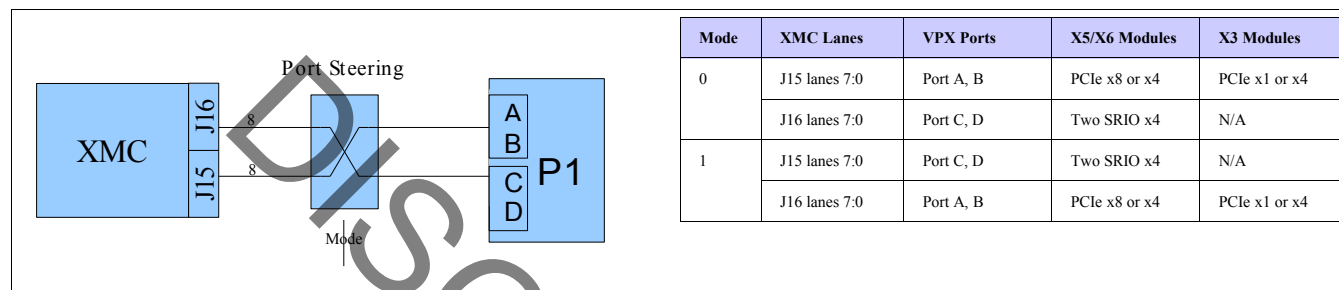
Models	
Air-cooled	Air flow-through design IEEE Std 1101.10 bracket and card ejector (same as compact PCI or VME) Optional REDI covers optional card locks
Conduction-cooled	Typical power dissipation is 25W from module to chassis with 15C temperature gradient Conduction cooling frame between XMC and adapter card Cooling frame contacts VITA20 thermal pattern and XMC hot components (thermal pads required) Frame clamps to enclosure with card locks Clamping force > 200N (both edges) Optional REDI covers Built-in card ejectors

XMC Adapter for 3U OpenVPX

Applications Information

XMC to VPX Port Mapping

The XMC communications ports are steered to the VPX backplane ports by configuring switches. This allows the XMC ports on J15 and J16 to connect to VPX ports A,B,C and D to match the backplane and application requirements.



The Innovative X5, X6 and X3 module families are compatible with several OpenVPX slot profiles.

Module Family	Modules	PCIe Lanes	Endpoints	Adapter Mode	XMC Configuration	OpenVPX Profile	Notes
X3	X3-SD, X3-SDF, X3-Servo, X3-A4D4, X3-SD16, X3-25M, X3-10M	x1, Gen1	1	0	Standard	MOD3-PER-1U-16.3.3.1	
	X3-2M, X3-DIO	x4, Gen1	1	0	Standard	MOD3-PAY-1F-16.3.2.1	
X5	All	x8, Gen1	1	0	Standard	MOD3-PAY-1D-16.2.6.1	
		x4, Gen1	1	0	x4 PCIe core	MOD3-PAY-1F-16.3.2.1	Standard for Matlab BSP.
X6	All	x8, Gen2	1	0	Standard	MOD3-PAY-1D-16.2.6.2	Also supports Gen1 MOD3-PAY-1D-16.2.6.1
		x4, Gen2	1	0	x4 PCIe core	MOD3-PAY-1F-16.3.2.2	Standard for Matlab BSP. Also supports Gen1 MOD3-PAY-1F-16.3.2.1
		x4, Gen2	2	0 or 1	Dual x4 PCIe cores	MOD3-PAY-2F-16.3.2.2	Requires custom logic. Also supports Gen1 MOD3-PAY-2F-16.3.2.1

Digital IO Mapping

The digital IO from the XMC is mapped to P2 from either J16 or Jn4, selected by on-card jumpers. The IO may be up to 3.3V. All digital IO connections are matched-length, differential pairs.

Mode	DIO	Mapping
0	Jn4	P64s
1	J16	X38s

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P2 Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1		GND	Jn4-1	Jn4-3	GND	Jn4-2	Jn4-4
2	GND	Jn4-5	Jn4-7	GND	Jn4-6	Jn4-8	GND
3		GND	Jn4-9	Jn4-11	GND	Jn4-10	Jn4-12
4	GND	Jn4-13	Jn4-15	GND	Jn4-14	Jn4-16	GND
5		GND	Jn4-17	Jn4-19	GND	Jn4-18	Jn4-20
6	GND	Jn4-21	Jn4-23	GND	Jn4-22	Jn4-24	GND
7		GND	Jn4-25	Jn4-27	GND	Jn4-26	Jn4-28
8	GND	Jn4-29	Jn4-31	GND	Jn4-30	Jn4-32	GND
9		GND	Jn4-33	Jn4-35	GND	Jn4-34	Jn4-36
10	GND	Jn4-37	Jn4-39	GND	Jn4-38	Jn4-40	GND
11		GND	Jn4-41	Jn4-43	GND	Jn4-42	Jn4-44
12	GND	Jn4-45	Jn4-47	GND	Jn4-46	Jn4-48	GND
13		GND	Jn4-49	Jn4-51	GND	Jn4-50	Jn4-52
14	GND	Jn4-53	Jn4-55	GND	Jn4-54	Jn4-56	GND
15		GND	Jn4-57	Jn4-59	GND	Jn4-58	Jn4-60
16	GND	Jn4-61	Jn4-63	GND	Jn4-62	Jn4-64	GND

XMC Jn4 to P2 Mapping (Mode 0)

P2 Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1		GND		GND	Jn6-F2	Jn6-F1	
2	GND	Jn6-F4	Jn6-F3	GND	Jn6-C2	Jn6-C1	GND
3		GND	Jn6-F6	Jn6-F5	GND	Jn6-C4	Jn6-C3
4	GND	Jn6-F8	Jn6-F7	GND	Jn6-C6	Jn6-C5	GND
5		GND	Jn6-F10	Jn6-F9	GND	Jn6-C8	Jn6-C7
6	GND	Jn6-F12	Jn6-F11	GND	Jn6-C10	Jn6-C9	GND
7		GND	Jn6-F14	Jn6-F13	GND	Jn6-C12	Jn6-C11
8	GND	Jn6-F16	Jn6-F15	GND	Jn6-C14	Jn6-C13	GND
9		GND	Jn6-F18	Jn6-F17	GND	Jn6-C16	Jn6-C15
10	GND	Jn6-C19	Jn6-F19	GND	Jn6-C18	Jn6-C17	GND

XMC J6 to P2 Mapping (Mode 1)

Power to the XMC Module

The XMC site provides +3.3V, +12V and -12V to the module. The VPWR pins are connected to either 5V or 12V as selected by an on-card jumper.

The power is sourced from the VPX backplane. Consult your system documentation to determine the maximum power available in the slot.

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XMC Supply Voltage	Maximum Current	Source
3.3V	6A	VPX backplane
+12V	3.3A	VPX backplane
-12V	0.1A	VPX backplane (-12VAUX)
VPWR (5V or +12V, jumper selectable)	5V @ 6A or 12V @ 3.3A	VPX backplane

Power Supplies to the XMC

Cooling the XMC Module

The VPX-XMC has both air-cooled and conduction-cooled adapter versions. Both versions are available with optional REDI covers for 2-Level Maintenance support.

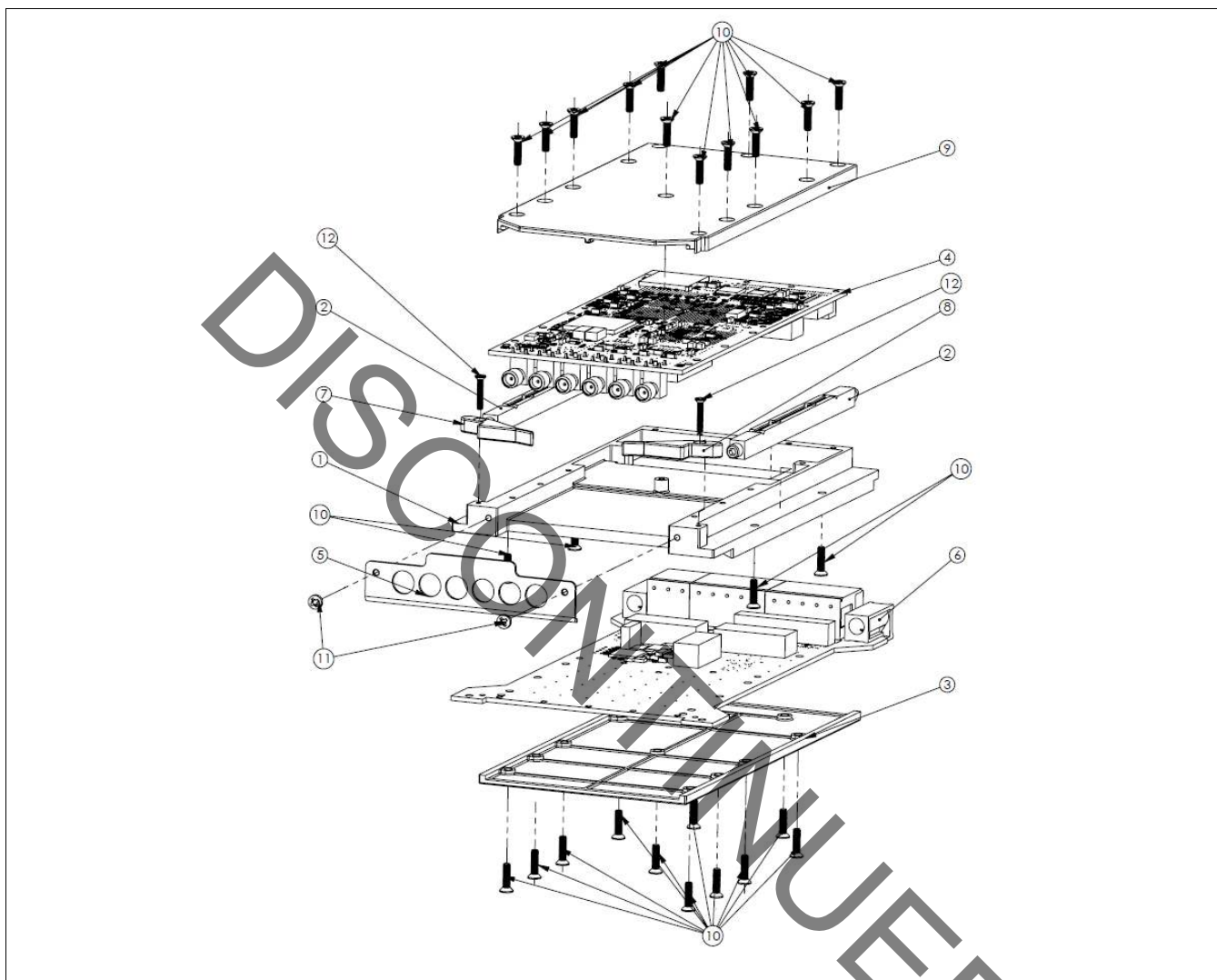


XMC-VPX Adapter



The conduction cooled adapter is designed to conduct heat from the XMC module using middle frame assembly to the outer rails that clamp to the case. All mechanicals conform to VITA 48.2 specification and support 0.8 in card spacing. The frame assembly form-fits the XMC module so that with the addition of thermal pads or grease, heat is transferred effectively to the frame and out to the chassis. The frame also attached to the VITA 20 conduction-cooling pattern on the XMC.

XMC Adapter for 3U OpenVPX



Exploded View of Conduction-Cooled VPX-XMC Adapter for X6 Modules

The air-cooled version of the adapter all conforms to VITA 48.1 specification. The adapter is designed to allow air flow across the short axis of the card from bottom to top. Air flow requirements should be assessed for each installation.

The adapter consumes less than 1W typically.

Triggering and Clock Inputs for Innovative X3 and X6 Families of I/O Modules

The adapter has special support that allows Innovative's X3 and X6 XMC IO module families to use backplane signals as triggers and clocks. These signals may be used for system synchronization and triggering such as simultaneous sampling across many modules with appropriate supporting logic in FPGA.

The system PPS and reference signals on VPX P0 connector map the XMC input. There are also signals map from the VPX P2 connector to the XMC module P16 connector.

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VPX Connector, Pins	Timing Signal	Direction	P16 Connection	Use
P2: A1/B1	XP16_CLK_P/N	Input	A9/B9	X3: sample clock input. X5: no connection X6: connects to MGTREFCLKP/N_112
P2: D1/E1	H_TRIG0_P/N	Input	A19	X3: DIO42, trigger input. X5: no connection X6: H_TRIG0 trigger input
P2: A3/B3	H_TRIG1_P/N	Input	B19	X3: DIO43, trigger input. X5: no connection X6: H_TRIG1 trigger input
P0: B8/C8	PPS_P/N	Input	D19	X3: DIO_CLK_P, PPS input. X5: no connection X6: PPS input
P0: E8/F8	REFCLK_25M_P/N	Input	D9/E9	VPX 25 MHz reference clock input. X3: may use as PLL reference for sample rate generation. X5: no connection X6: FPGA clock input FMC_CLKP/N

The two trigger inputs, H_TRIG0 and H_TRIG1, as well as PPS are converted from LVDS to LVCMOS on the adapter card. Voltage level must be set with jumper for 3.3V (X3 modules) or 2.5V (X6 modules).

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Mailing Address: Innovative Integration, Inc.

2390A Ward Avenue, Simi Valley, California 93065

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